SPECIFICATION

Docket No. **BA-00585**

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, **Bin Li**, a citizen of Canada, **Kenneth R. Knowles** and **David C. Lawson**, both citizens of the United States of America, all residing in the State of Virginia, have invented new and useful improvements in a

READ/WRITE CIRCUIT FOR ACCESSING CHALCOGENIDE NON-VOLATILE MEMORY CELLS

of which the following is a specification:

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to memory circuits in general, and in particular to memory circuits having chalcogenide cells. Still more particularly, the present invention relates to a read/write circuit for accessing chalcogenide memory cells.

2. Description of the Related Art

The use of electrically writable and erasable phase change materials for electronic memory applications is known in the art. Such phase change materials can be electrically switched between a first structural state where the material is generally amorphous and a second structural state where the material is generally crystalline. The phase change material exhibits different electrical characteristics depending upon its state. For example, in its amorphous state, the phase change material exhibits a lower electrical conductivity than it does in its crystalline state. The phase change material may also be electrically switched between different detectable states of local order across the entire spectrum ranging from the completely amorphous state to the completely crystalline state. In other words, the state switching of the phase change materials is not limited to either completely amorphous or completely crystalline states but rather in incremental steps to provide a "gray scale" represented by a multiplicity of conditions of local order spanning the spectrum from the completely amorphous state to the completely crystalline state.

General speaking, phase change material memory cells are monolithic, homogeneous, and formed of chalcogenide material containing chemical elements selected from the group of Tellurium (Te), Selenium (Se), Antimony (Sb), Nickel (Ni), and Germanium (Ge). Chalcogenide memory cells can be switched between two different electrically detectable states within nanoseconds in response to an input of picojoules of

energy. Chalcogenide memory cells are truly non-volatile and can maintain the stored information without the need for periodic refreshing. Furthermore, the stored information remain intact even when power is removed from the chalcogenide memory cells.

The present disclosure describe a read/write circuit for accessing chalcogenide memory cells.

SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the present invention, a non-volatile memory includes a chalcogenide storage element, a voltage limiting circuit, a current-to-voltage converter, and a buffer circuit. The voltage limiting circuit, which is coupled to the chalcogenide storage element, ensures that voltages across the chalcogenide storage element will not exceed a predetermined value during a read operation. During a read operation, the current-to-voltage converter, which is coupled to the voltage limiting circuit, converts a current pulse read from the chalcogenide storage element to a voltage pulse. By sensing the voltage pulse from the current-to-voltage converter, the buffer circuit can determine a storage state of the chalcogenide storage element.

All objects, features, and advantages of the present invention will become apparent in the following detailed written description.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention itself, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure **1** is a block diagram of a static random access memory, according to the prior art;

Figure **2** is a block diagram of a chalcogenide random access memory, in accordance with a preferred embodiment of the present invention;

Figure **3** is a circuit diagram of a write circuit for writing data to the chalcogenide random access memory from Figure **2**, in accordance with a preferred embodiment of the present invention; and

Figure **4** is a circuit diagram of a read circuit for reading data from the chalcogenide random access memory from Figure **2**, in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to the drawings and in particular to Figure **1**, there is illustrated a block diagram of a static random access memory (SRAM), according to the prior art. As shown, a SRAM **10** includes a storage element **11** coupled to a sense amplifier **12**. Data in and out of storage element **11** are controlled by a wordline switch **13**. Storage element **11** is commonly made of cross-coupled inverters, as it is well-known to those skilled in the art. During a write operation, writeline switch **13** turns on a corresponding wordline to allow data to be written into storage element **11**. During a read operation, the data stored within storage element **11** is read via sense amplifier **12**. A major drawback of SRAM **10** is that data stored in storage element **11** will be lost if the power to SRAM **10** is momentarily interrupted.

With reference now to Figure **2**, there is depicted a block diagram of a chalcogenide random access memory (CRAM), in accordance with a preferred embodiment of the present invention. As shown, a CRAM **20** includes a chalcogenide storage element **26** and a wordline switch **27**. As its name implies, chalcogenide storage element **26** includes a memory cell formed of chalcogenide material containing chemical elements selected from the group of Tellurium (Te), Selenium (Se), Antimony (Sb) and Germanium (Ge). In addition, CRAM **20** also includes various circuits for accessing chalcogenide storage element **26**, such as a current mirror **21**, a buffer **22**, a current-voltage converter **23**, a voltage limiting circuit **24** and a bitline switch **25**.

Referring now to Figure **3**, there is depicted a circuit diagram of a write circuit for writing data to CRAM **20**, in accordance with a preferred embodiment of the present invention. As shown, a write circuit **30** includes a write control circuit **31**, a row decoder **32** and a write current supply circuit **33**. Write control circuit **31** receives three separate inputs, namely, a write_enable input, a col_write input and a data_in input. In turn, write control circuit **31** generates a first output **34** and a second output **35** for

controlling the gate of a p-channel transistor **P3** and the gate of a p-channel transistor **P4**, respectively, within write current supply circuit **33**. The drains of transistors **P3** and **P4** are connected to a power supply V_{DD}. The sources of transistors **P3** and **P4** are connected to chalcogenide storage element **26**. Chalcogenide storage element **26** is connected to ground via a row pass n-channel transistor **N1**. Row decoder **32** receives an address input and a clock input for controlling the gate of row pass transistor **N1**.

Under the control of write control circuit **31**, write current supply circuit **33** writes data to chalcogenide storage element **26**. When the write_enable input to write control circuit **31** is at a logical high, and the col_write input to write control circuit **31** is also at a logical high because of a selected address, either p-channel transistor **P3** or p-channel transistor **P4** within write current supply circuit **33** will be turned on, depending on whether the data at the data_in input to write control circuit **31** is at a logical high or a logical low. In the meantime, with the selected address, row pass transistor **N1** is turned on when the clock signal to row decoder **32** is at a logical high. Since row pass transistor **N1** is turned on and either p-channel transistor **P3** or p-channel transistor **P4** is also turned on, a certain amount of current begins to flow through chalcogenide storage element **26**, which makes chalcogenide storage element **26** change its phase, either from an amorphous phase to a crystalline phase or from a crystalline phase to an amorphous phase. The required current for chalcogenide storage element **24** to reach an amorphous phase and a crystalline phase are preferably 1 mA and 0.5 mA, respectively.

With reference now to Figure **4**, there is depicted a circuit diagram of a read circuit for reading data from CRAM **20**, in accordance with a preferred embodiment of the present invention. As shown, a read circuit **40** includes a read control circuit **43**, row decoder **32** and a current-to-voltage converter circuit **42**. Read control circuit **43** receives two separate inputs, namely, a read_enable input and an address_column input. In turn, read control circuit **41** generates a column_read signal for controlling the gate of a column read pass n-channel transistor **N2**. A p-channel transistor **P1**, an n-channel transistor **N3**,

n-channel transistor **N2**, chalcogenide storage element **26** and an n-channel transistor **N4** are connected between power supply V_{DD} and ground.

Current-to-voltage converter circuit **42** includes a p-channel transistor **P2**, an n-channel transistor **N4** and an inverter **I1**. Current-to-voltage converter circuit **42** generates a data output signal via a buffer **22**. Row decoder **32** receives an address input and a clock input for controlling the gate of row pass n-channel transistor **N4**.

Under the control of read control circuit **43**, current-to-voltage converter circuit **42** reads data from chalcogenide storage element **26**. When the read_enable input to read control circuit **43** is at a logical high and the address_column input to read control circuit **43** is also at a logical high because of a selected address to row decoder **32**, column read pass transistor **N2** is turned on. Row pass transistor **N4** is also turned on once both the selected address input and clock input to row decoder **32** are at a logical high.

Since both column read pass transistor **N2** and row pass transistor **N4** are turned on, the current should flow from V_{DD} through transistor **P1**, transistor **N3**, transistor **N2**, chalcogenide storage element **24**, and transistor **N4** to ground, which generates a current pulse. The amplitude of the generated current pulse is determined by the phase of chalcogenide storage element **26**. The conductive state of chalcogenide storage element **26** is then sensed and converted to a voltage pulse by current-to-voltage converter circuit **42**. The voltage pulse is then bufferred out by buffer circuit **22**. The voltage across chalcogenide storage element **26** is strictly limited because of a predetermined V_limit applied to the gate of transistor **N3**.

There are two important constraints on a read operation: first, the voltage across chalcogenide storage element **26** cannot exceed a threshold voltage level (otherwise, the phase of chalcogenide storage element **26** may be altered); and second, the read current

flow through chalcogenide storage element **26** should be smaller than the value that could change the phase of chalcogenide storage element **26**.

As has been described, the present invention provides a read/write circuit for accessing a single chalcogenide memory cell. Although only one chalcogenide storage element is utilized to illustrate the present invention, it is understood by those skilled in the art that two chalcogenide storage elements can be associated with a logical data bit by utilizing a double-ended or "differential" version of the above-described single-ended circuit. The doubled-end circuit is similar to the above-described single-ended circuit except that there is a complementary data input with its own read and write circuits to store the complement of each input data bit in a chalcogenide storage element, and a differential amplifier circuit is utilized to sense the complementary data bits stored. The differential design of the true-and-complement value of each logical data bit provides a higher noise margin and thus provides a greater reliability for each data bit stored in case of a defect exists in the input signals or the chalcogenide memory chip.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.